TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS017

# CD4006B Types

## CMOS 18-Stage Static Shift Register

High-Voltage Types (20-Volt Rating)

■ CD4006B types are composed of 4 separate shift register sections: two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent single-rail data path.

A common clock signal is used for all stages. Data are shifted to the next stage on negative-going transitions of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, 17 and 18 stages can be implemented using one CD4006B package. Longer shift register sections can be assembled by using more than one CD4006B.

To facilitate cascading stages when clock rise and fall times are slow, an optional output ($D_1$+4') that is delayed one-half clock-cycle, is provided (see Truth Table for Output from Term. 2).

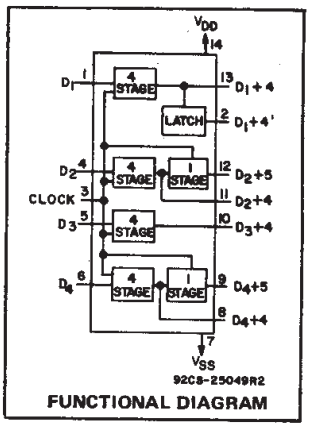
The CD4006B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

*Features:*

- Fully static operation
- Shifting rates up to 12 MHz @ 10 V (typ.)
- Permanent register storage with clock line high or low — no information recirculation required
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at $V_{DD}$ = 5 V; 2 V at $V_{DD}$ = 10 V; 2.5 V at $V_{DD}$ = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

*Applications:*

- Serial shift registers
- Frequency division
- Time delay circuits




FUNCTIONAL DIAGRAM

TRUTH TABLE FOR SHIFT REGISTER STAGE

| D | CL▲ | D + 1 |
|---|---|---|
| 0 | ↓ | 0 |
| 1 | ↓ | 1 |
| X | ↓ | NC |

TRUTH TABLE FOR OUTPUT FROM TERM.2

| $D_1$+4 | CL▲ | $D_1$+4' |
|---|---|---|
| 0 | ↑ | 0 |
| 1 | ↑ | 1 |
| X | ↓ | NC |

1 = HIGH; 0 = LOW; NC = NO CHANGE; X = DON'T CARE; ▲ = LEVEL CHANGE

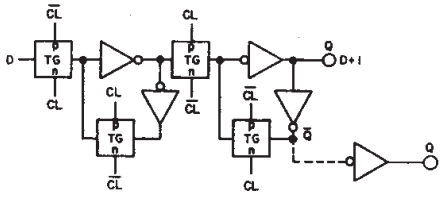
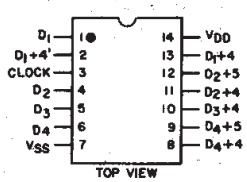
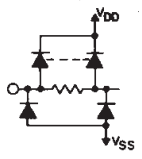



*Fig. 1 — Logic diagram and truth table (one register stage).*

**TERMINAL ASSIGNMENT**




ALL INPUTS (TERMINALS 1,3,4,5,6) PROTECTED BY CMOS PROTECTION NETWORK

92CS-28974

**RECOMMENDED OPERATING CONDITIONS at $T_A$ = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | $V_{DD}$ (V) | LIMITS Min. | LIMITS Max. | UNITS |
|---|---|---|---|---|
| Supply-Voltage Range (For $T_A$ = Full Package Temperature Range) | – | 3 | 18 | V |
| Clock Pulse Width, $t_W$ | 5 | 180 | – | ns |
| | 10 | 80 | – | |
| | 15 | 50 | – | |
| Data Setup Time, $t_S$ | 5 | 100 | – | ns |
| | 10 | 50 | – | |
| | 15 | 40 | – | |
| Data Hold Time, $t_H$ | 5 | 60 | – | ns |
| | 10 | 40 | – | |
| | 15 | 30 | – | |
| Clock Rise or Fall Time: $t_r$, $t_f$ | 5,10, 15 | – | 15 | μS |
| Clock Input Frequency, $f_{CL}$ | 5 | – | 2.5 | MHz |
| | 10 | – | 5 | |
| | 15 | – | 7 | |

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
(Voltages referenced to $V_{SS}$ Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to $V_{DD}$ +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -55°C to +100°C ..... 500mW
For $T_A$ = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW
OPERATING-TEMPERATURE RANGE ($T_A$) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE ($T_{stg}$) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

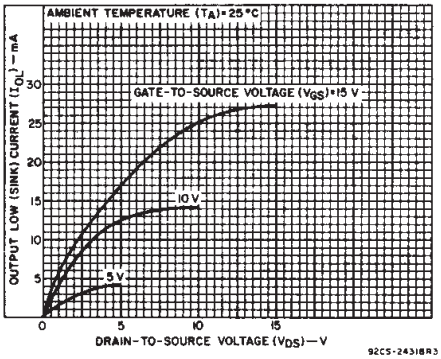



*Fig. 2 – Typical output low (sink) current characteristics.*

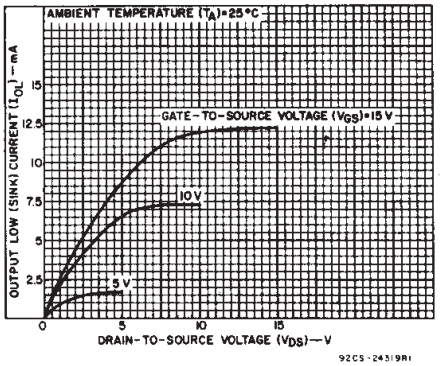



*Fig. 3 – Minimum output low (sink) current characteristics.*

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | +25 | | | |
| | $V_O$ (V) | $V_{IN}$ (V) | $V_{DD}$ (V) | -55 | -40 | +85 | +125 | Min. | Typ. | Max. | |
| Quiescent Device Current, $I_{DD}$ Max. | – | 0,5 | 5 | 5 | 5 | 150 | 150 | – | 0.04 | 5 | μA |
| | – | 0,10 | 10 | 10 | 10 | 300 | 300 | – | 0.04 | 10 | |
| | – | 0,15 | 15 | 20 | 20 | 600 | 600 | – | 0.04 | 20 | |
| | – | 0,20 | 20 | 100 | 100 | 3000 | 3000 | – | 0.08 | 100 | |
| Output Low (Sink) Current $I_{OL}$ Min. | 0.4 | 0,5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | – | mA |
| | 0.5 | 0,10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | – | |
| | 1.5 | 0,15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3 4 | 6.8 | – | |
| Output High (Source) Current, $I_{OH}$ Min. | 4.6 | 0,5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | – | |
| | 2.5 | 0,5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | – | |
| | 9.5 | 0,10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | – | |
| | 13.5 | 0,15 | 15 | -4.2 | -4 | -2.8 | -2.4 | -3.4 | -6.8 | – | |
| Output Voltage: Low-Level, $V_{OL}$ Max. | – | 0,5 | 5 | 0.05 | | | | – | 0 | 0.05 | V |
| | – | 0,10 | 10 | 0.05 | | | | – | 0 | 0.05 | |
| | – | 0,15 | 15 | 0.05 | | | | – | 0 | 0.05 | |
| Output Voltage: High-Level, $V_{OH}$ Min. | – | 0,5 | 5 | 4.95 | | | | 4.95 | 5 | – | |
| | – | 0,10 | 10 | 9.95 | | | | 9.95 | 10 | – | |
| | – | 0,15 | 15 | 14.95 | | | | 14.95 | 15 | – | |
| Input Low Voltage, $V_{IL}$ Max. | 0.5, 4.5 | – | 5 | 1.5 | | | | — | — | 1.5 | V |
| | 1, 9 | – | 10 | 3 | | | | — | — | 3 | |
| | 1.5,13.5 | – | 15 | 4 | | | | — | — | 4 | |
| Input High Voltage, $V_{IH}$ Min. | 0.5, 4.5 | – | 5 | 3.5 | | | | 3.5 | — | — | |
| | 1, 9 | – | 10 | 7 | | | | 7 | — | — | |
| | 1.5,13.5 | - | 15 | 11 | | | | 11 | — | — | |
| Input Current $I_{IN}$ Max. | – | 0,18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | – | $\pm 10^{-5}$ | ±0.1 | μA |

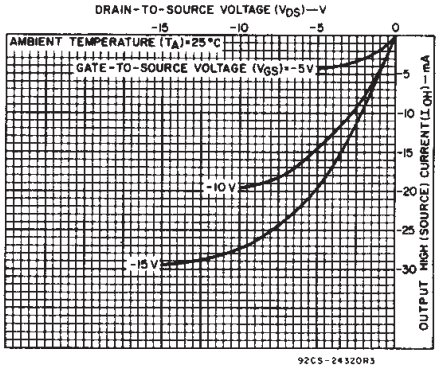



*Fig. 4 – Typical output high (source) current characteristics.*

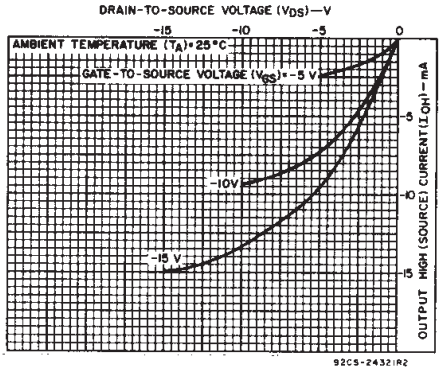



*Fig. 5 – Minimum output high (source) current characteristics.*

**DYNAMIC ELECTRICAL CHARACTERISTICS** *at $T_A$ = 25°C; Input $t_r$,$t_f$ = 20 ns, $C_L$ = 50 pF, $R_L$ = 200 kΩ*

| CHARACTERISTIC | TEST CONDITIONS $V_{DD}$ (V) | LIMITS MIN. | LIMITS TYP. | LIMITS MAX. | UNITS |
|---|---|---|---|---|---|
| Propagation Delay Time, $t_{PHL}$, $t_{PLH}$ | 5 | — | 200 | 400 | ns |
| | 10 | — | 100 | 200 | |
| | 15 | — | 80 | 160 | |
| Transition Time, $t_{THL}$, $t_{TLH}$ | 5 | — | 100 | 200 | ns |
| | 10 | — | 50 | 100 | |
| | 15 | — | 40 | 80 | |
| Minimum Data Setup Time, $t_s$ | 5 | — | 50 | 100 | ns |
| | 10 | — | 25 | 50 | |
| | 15 | — | 20 | 40 | |
| Minimum Clock Pulse Width, $t_w$ | 5 | — | 100 | 200 | ns |
| | 10 | — | 45 | 90 | |
| | 15 | — | 30 | 60 | |
| Maximum Clock Input Frequency, $f_{CL}$ | 5 | 2.5 | 5 | — | MHz |
| | 10 | 5 | 10 | — | |
| | 15 | 7 | 14 | — | |
| Maximum Clock Input Rise or Fall Time, $t_rCL$, $t_fCL$* | 5 | — | — | 15 | μs |
| | 10 | — | — | 15 | |
| | 15 | — | — | 15 | |
| Input Capacitance, $C_{IN}$ | Any Input | — | 5 | 7.5 | pF |

*If more than one unit is cascaded $t_rCL$ should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

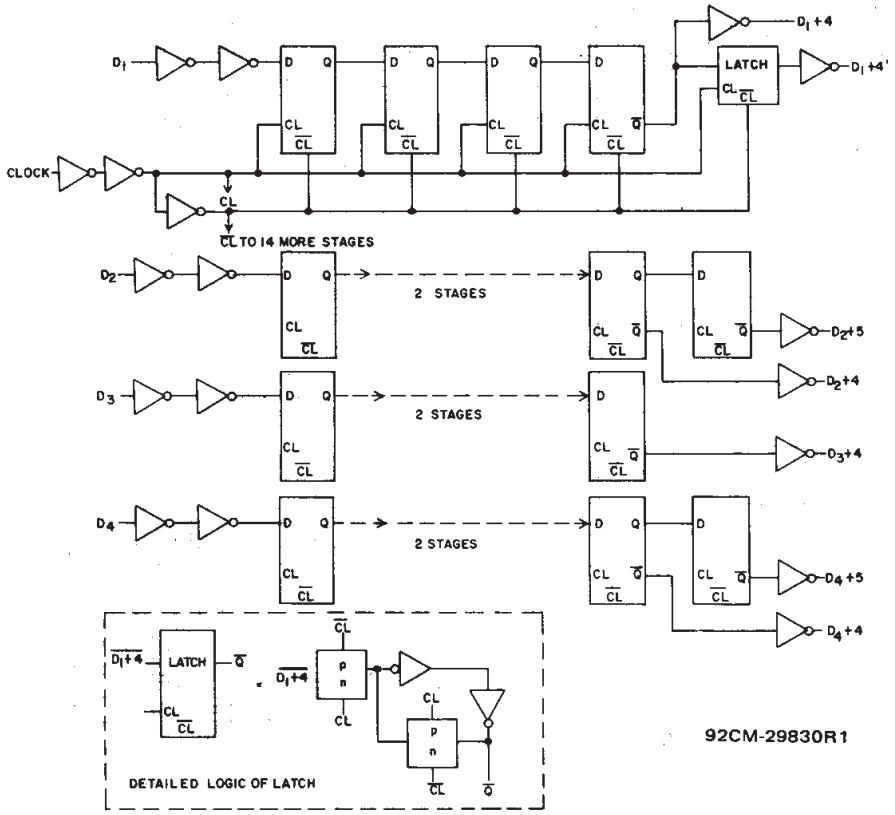



*Fig. 6 – Logic diagram with detail of latch.*

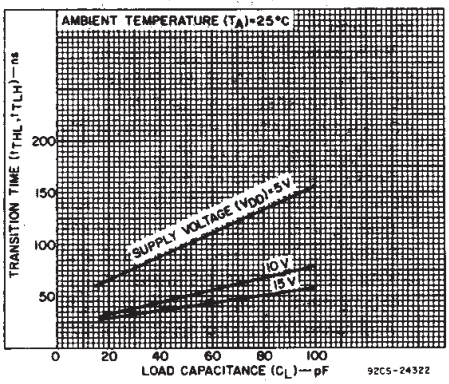



*Fig. 7 – Typical transition time as a function of load capacitance.*

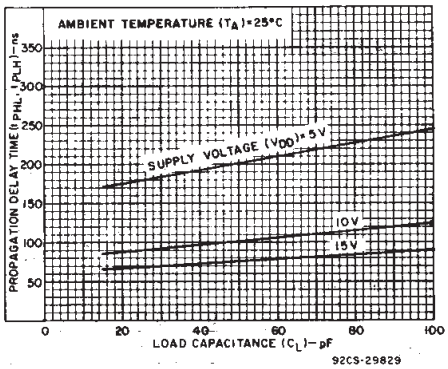



*Fig. 8 – Typical propagation delay time as a function of load capacitance.*

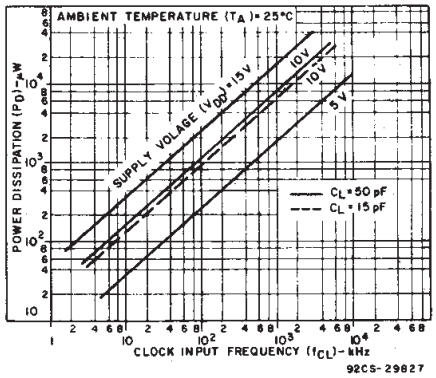



*Fig. 9 – Typical dyanamic power dissipation as a function of clock frequency.*

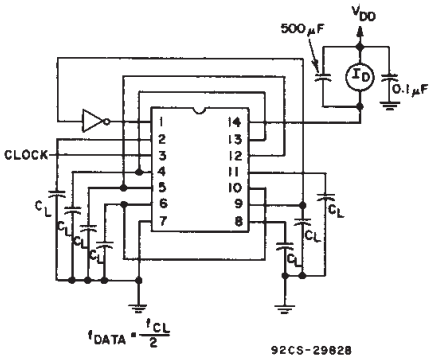



Fig. 10 – Dynamic power dissipation test circuit.

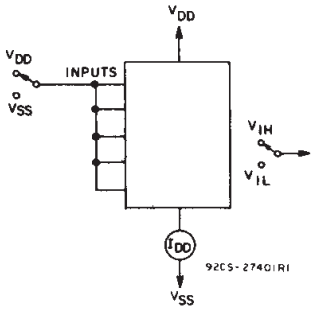



Fig. 11 – Quiescent device current test circuit.

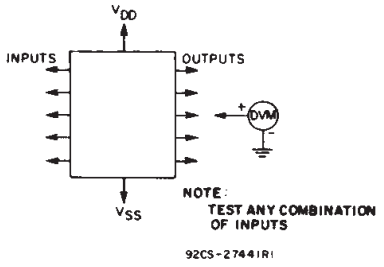



Fig. 12 – Input voltage test circuit.

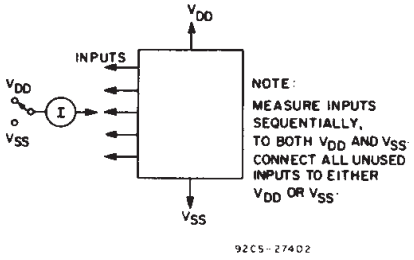
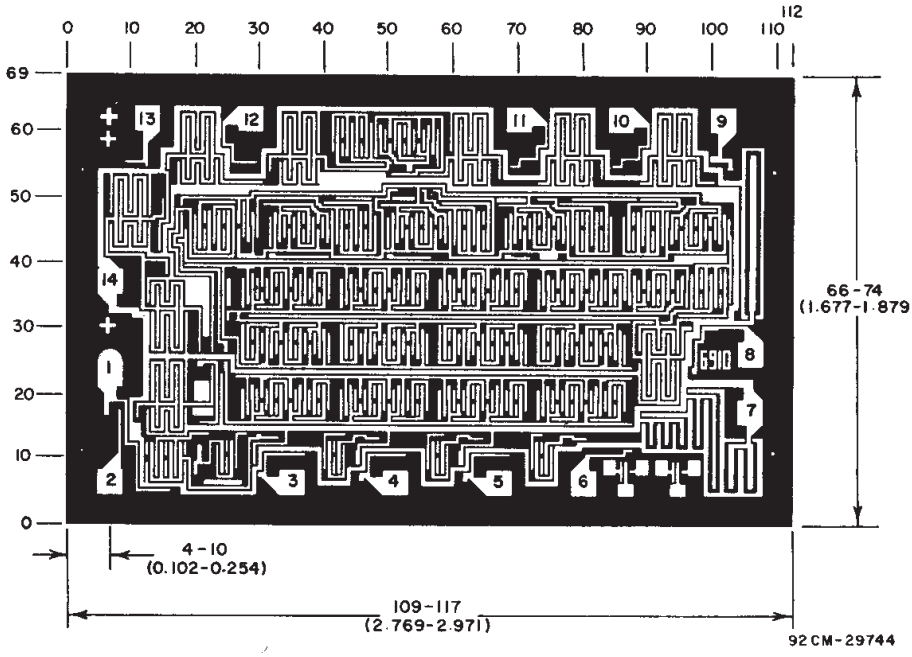



Fig. 13 – Input current test circuit.




*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ($10^{-3}$ inch).*

*Dimensions and pad layout for CD4006BH.*

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